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TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

NXP

LinkBo: A Single-Wire, Low-Latency, and Robust Protocol for Variable-Distance Chip-to-Chip Communications

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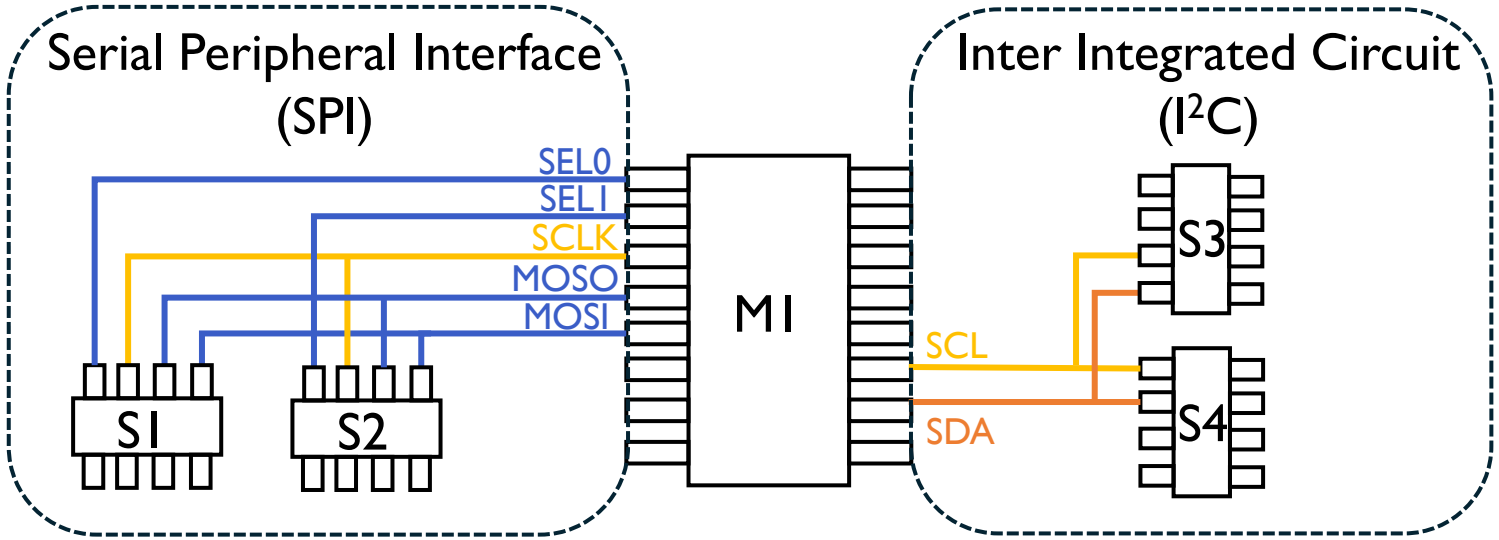
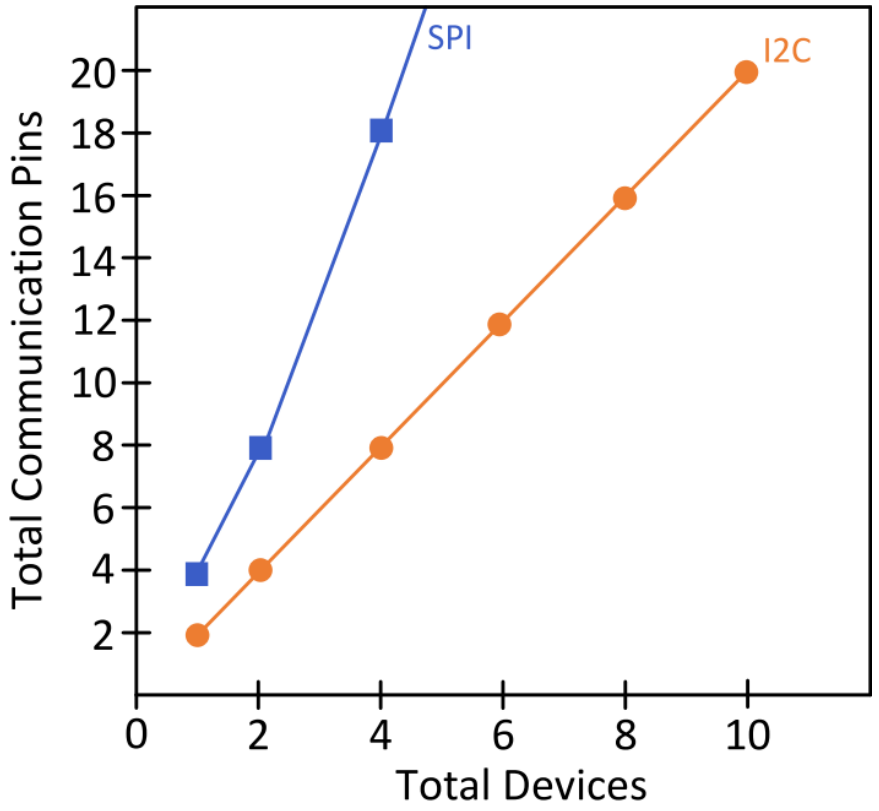
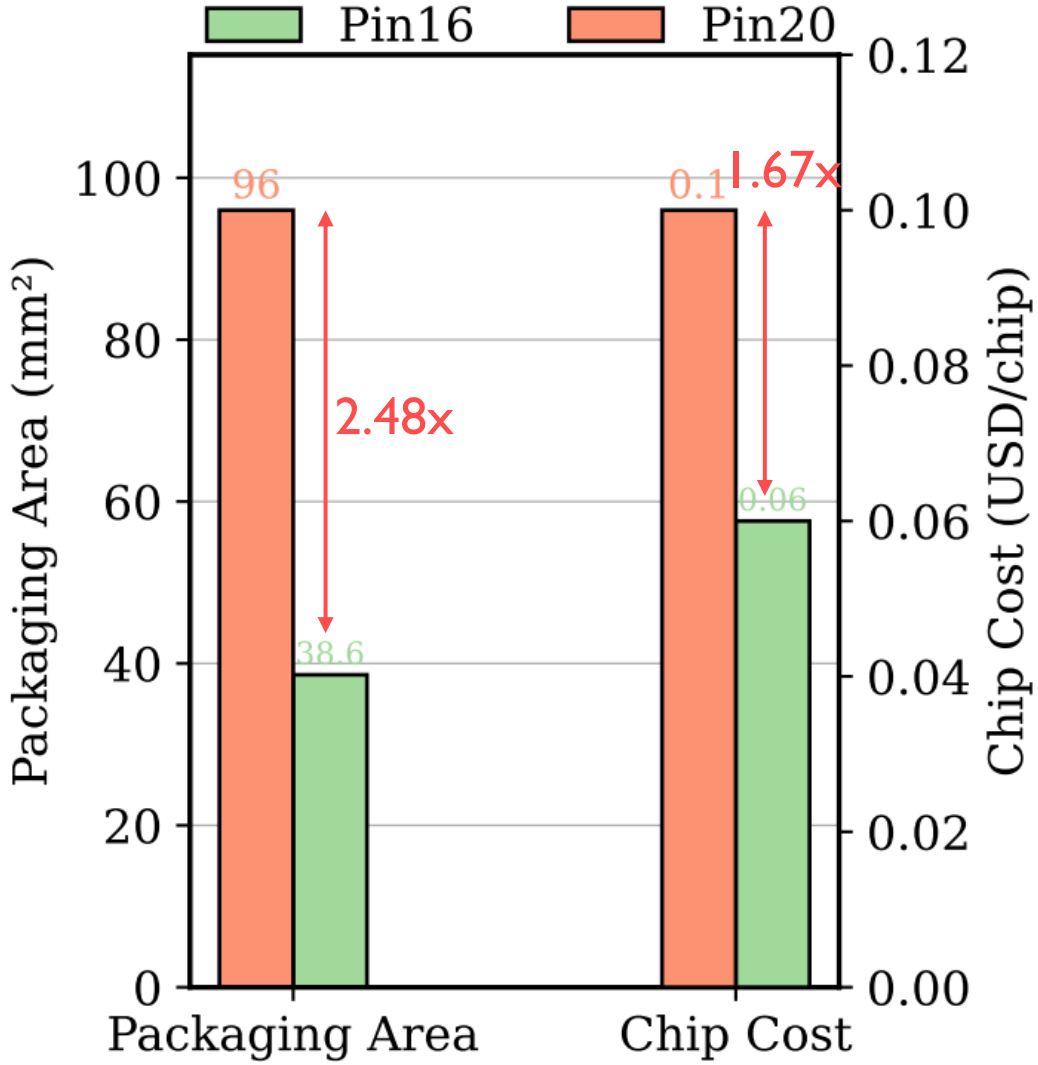
Pin-Efficiency Chip-to-Chip Communication?

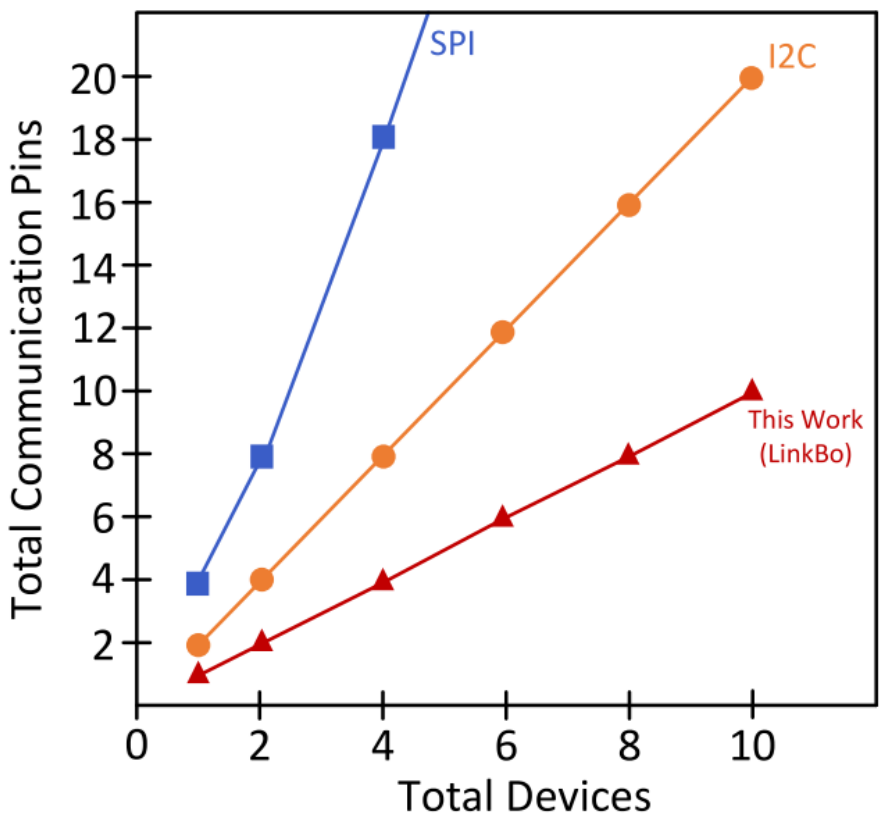


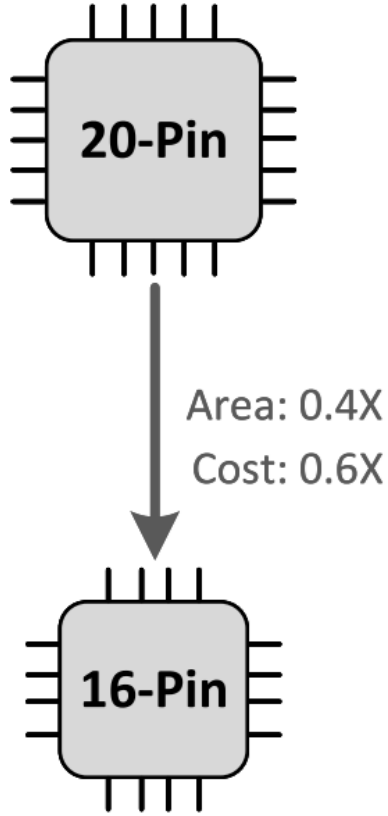


SPI and I2C use too much Pin count !

Why fewer Pins matter?





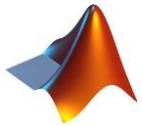


Pin count cause high cost and area !

Contributions of our work

LinkBo

Protocol: Single Wire | Low Latency | Robust | Chip-to-Chip

System Model: Performance Analysis |  | Real Channel Simulation

Hardware: FPGA demo | AMD XILINX | Variable-distance | Async Communication

Outline

01

Motivation

Chip-to-Chip communication and pin count optimization

02

Background & Related Work

State-of-the-art and scope for improvements

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LinkBo Protocol

Proposed single-wire protocol and system model evaluation

04

Hardware Architecture

Propsed LinkBo hardware architecture (TX, RX, Driver)

05

Results

Experimental evaluation of proposed designs

06

Conclusions

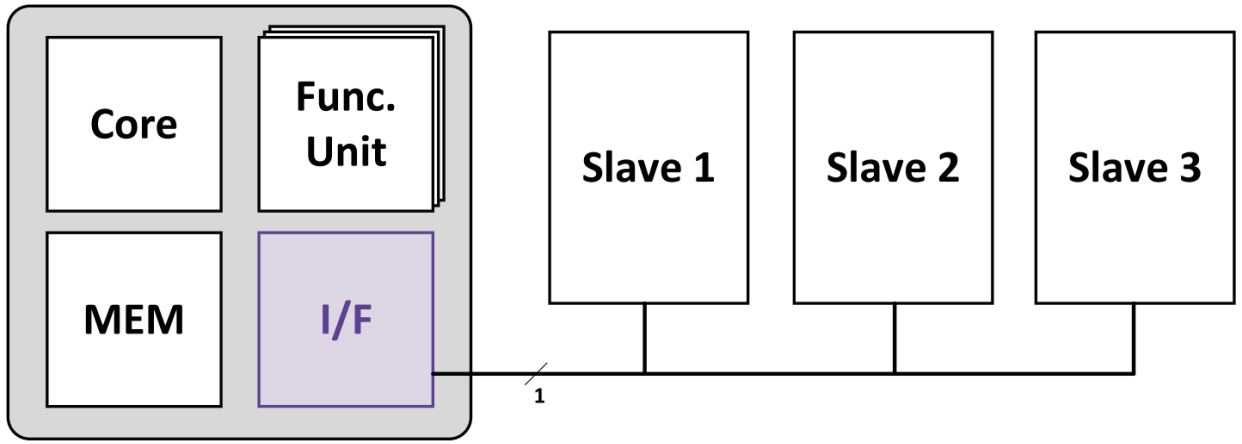
Summary and scope for related future research

Background & Related Wors

- 1-Wire Protocol
- Async communication Code

1-wire Protocol (ADI)

Basic Operations:
1. Reset: 960 μs
2. Write Bit 0: 70 μs
3. Write Bit 1: 70 μs
4. Read Bit: 70 μs



① Reset Pulse: 960 μs
② Devices Select Message:

8-bit Family Code	48-bit Address Code	8-bit CRC

③ Command Message :

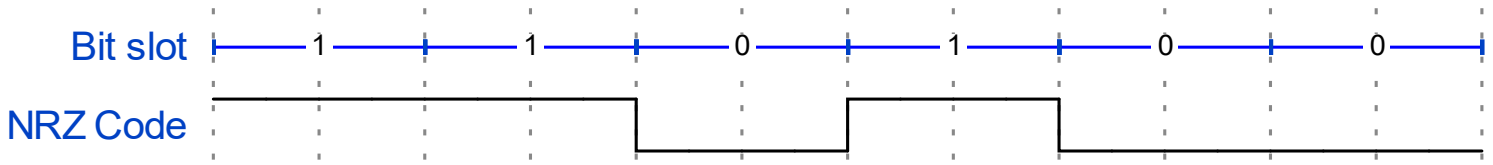
16-bit Command (ROM Function)	64-bit Data

Cons:
Only One Host
Low Bitrate / High Latency

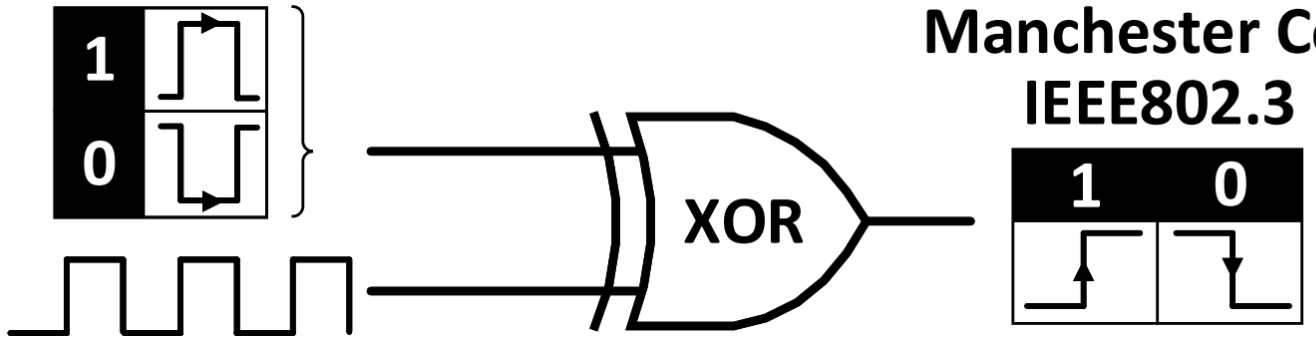
Pros: One Pin
Long Distance

Current 1-wire protocol has very long bit slot !

Asynchronous communication Code



Non-Return-to-Zero (NRZ) Code
(1-wire protocol)



Manchester Code
Pros:
Self-clocking, Robust to interference,
Simple implementation

Manchester code is better for Asynchronous Communication !

Commercial Product

Protocol	1-wire (TI[1],ADI)	UNI/O (MicroChip[2])	SWIM[3] /debugWIRE
Sync/Async	Async	Async	Async
Speed	8.33-111 kbps	10-100 kbps	10kbps-1Mbps
Type	Master/slave	Master/slave	Point to Point
Duplex	Half	Half	Half
Pin count	1	1	1
Application	EEPROM, Sensor	EEPROM, Sensor	Debug system

Limitations:

- Bit slot and reset use too much time
- No ACK or Every 8-bit with 2-bit ACK.
- Can't check error
- Only one host control bus

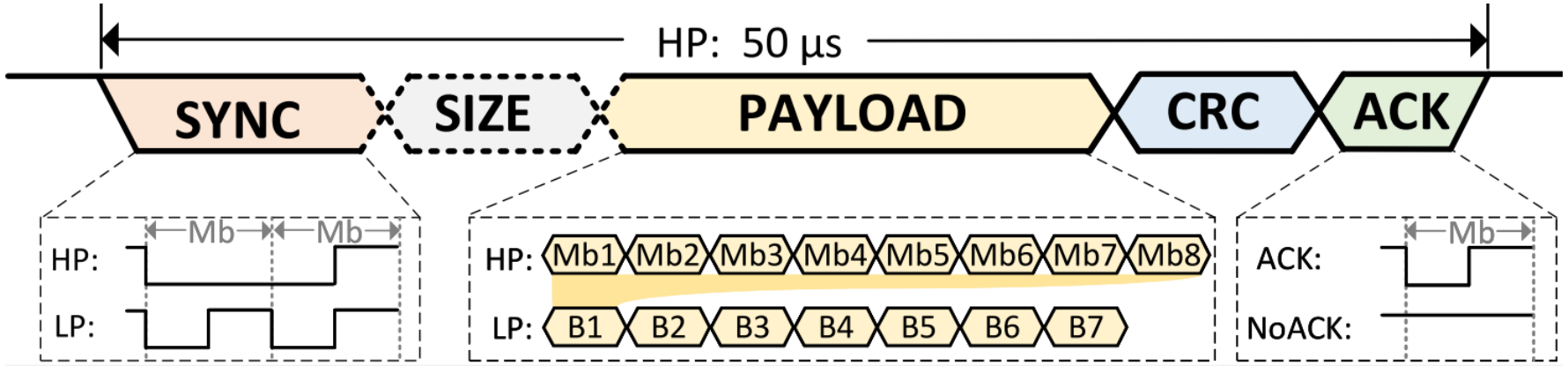
Commercial product still have low bitrate and high latency !

[1] UNI/O Bus Sepecification. 2009. URL: https://ww1.microchip.com/downloads/aemDocuments/documents/OTH/ProductDocuments/ReferenceManuals/22076D.pdf. [3]STMicroelectronics NV. STM8 SWIM communication protocol and debug module. 2016. URL: https://www.st.com/resource/en/usermanual/um0470-stm8-swim-communication-protocol-and-debug-module-stmicroelectronics.pdf#page=8.10.

LinkBo Protocol

- Protocol Definition
- System Model

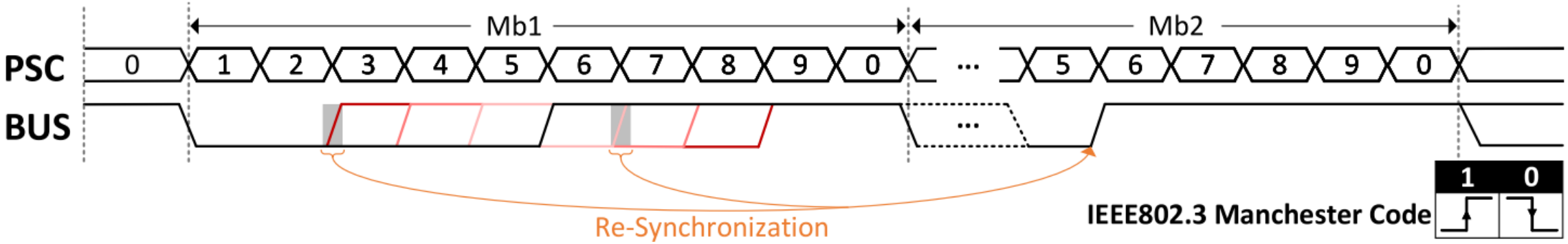
Protocol Definition



- **Priority**
  - High Priotiy (HP) / Low Priotity (LP)
- **SYNC**
  - 2 Manchester bits (Mbs)
  - Different SYNC for different priority
- **SIZE**
  - Only LP has SIZE field
  - 3 Manchester bits (Mbs)
- **PALOAD**
  - HP have 8 Mbs
  - LP can support up to 7 Byte (7*8 Mbs)
- **CRC**
  - 4 bits CRC for each HP/LP message
- **ACK**
  - 1 Manchester bits (Mbs)
  - RX send back ACK

Reduce Manchester slot and add 2 priority messages

Re-Synchronization

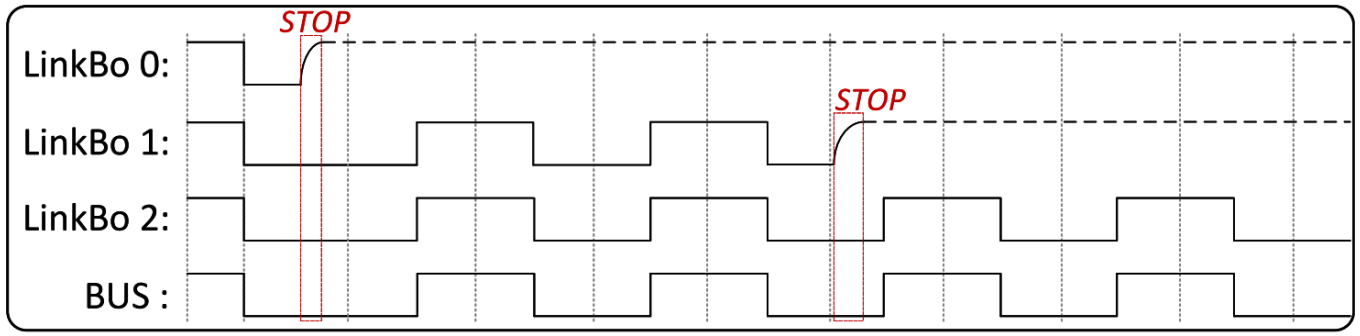


- Important for variable-distance communication
  - Because longer wires introduce more distortion and skew

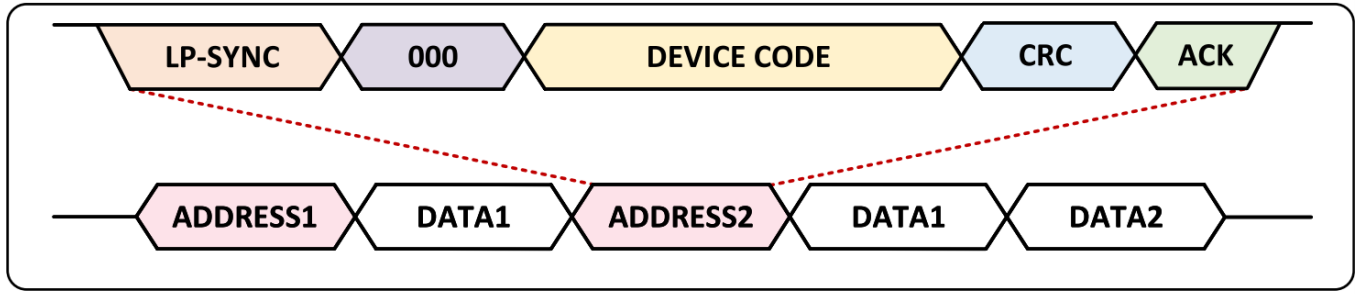
- Simple mechanism
  - Only need a prescaler counter (PSC) to count the cycle of Manchester bit slot.

Make sure every transition edge at middle of Manchester slot

Scalability for multi-device



(a)



(b)

Wire-AND logic

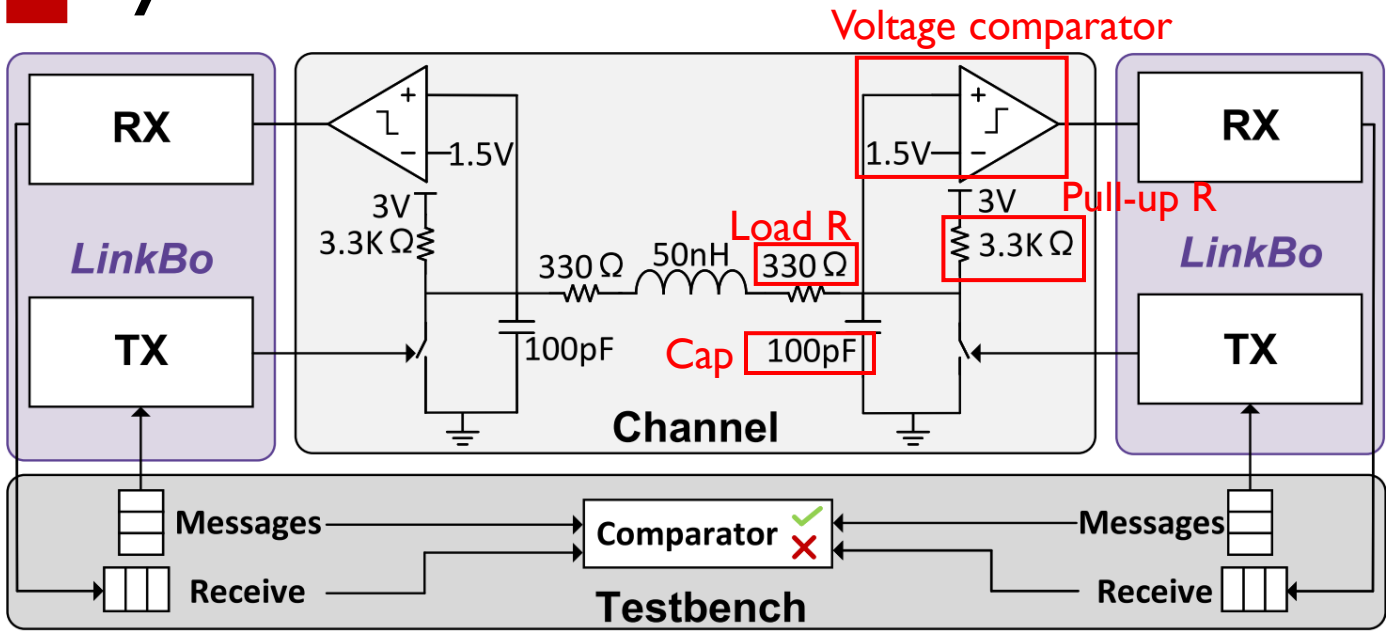
- First high signal will lose arbitration

Multi-device:

- SIZE=000
- Fist message carry 8-Mb device code
- Second message carry real data

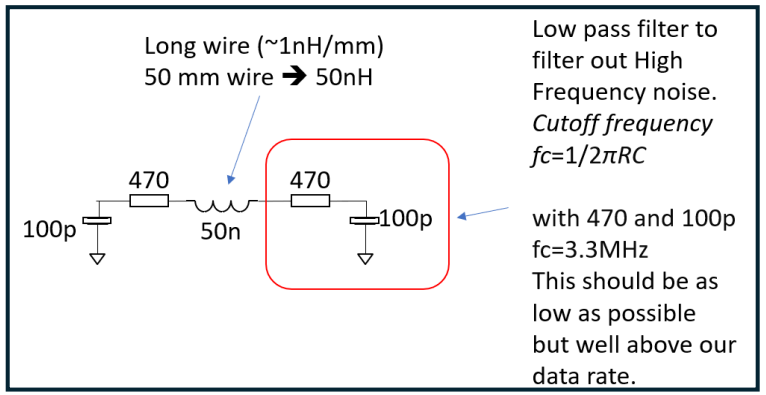
Support multi-device transmission theoretically

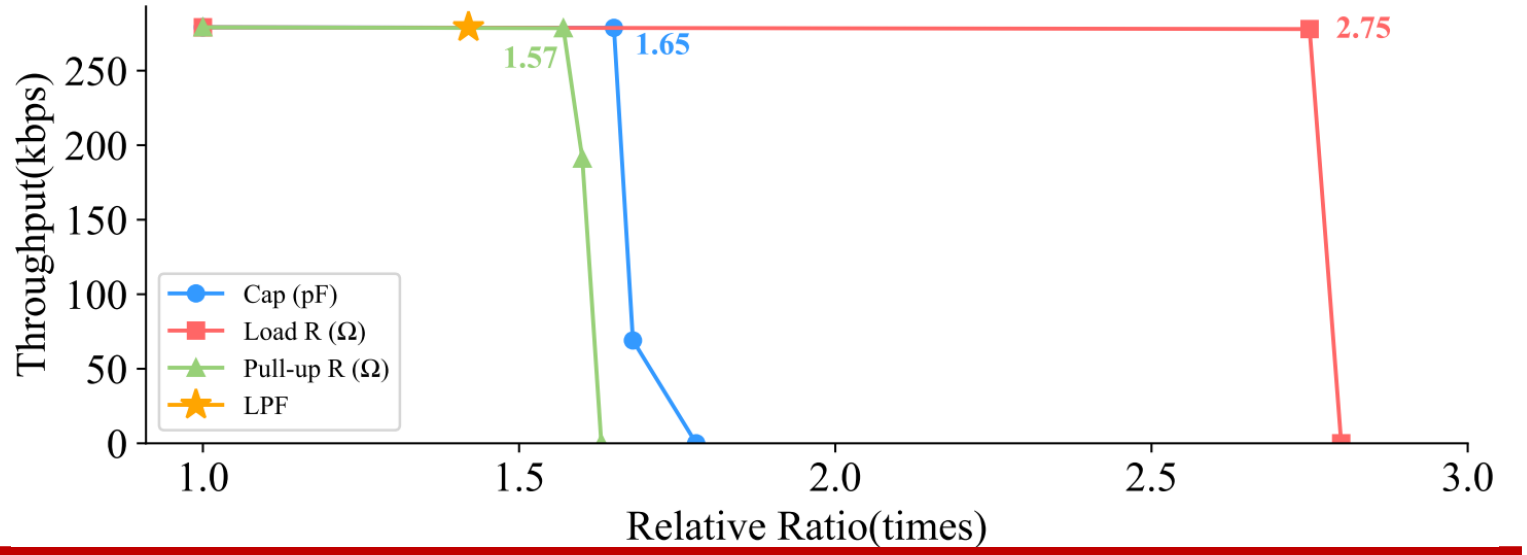
System Model



Simulate the real parameter of PCB !

★: Low pass filter condition

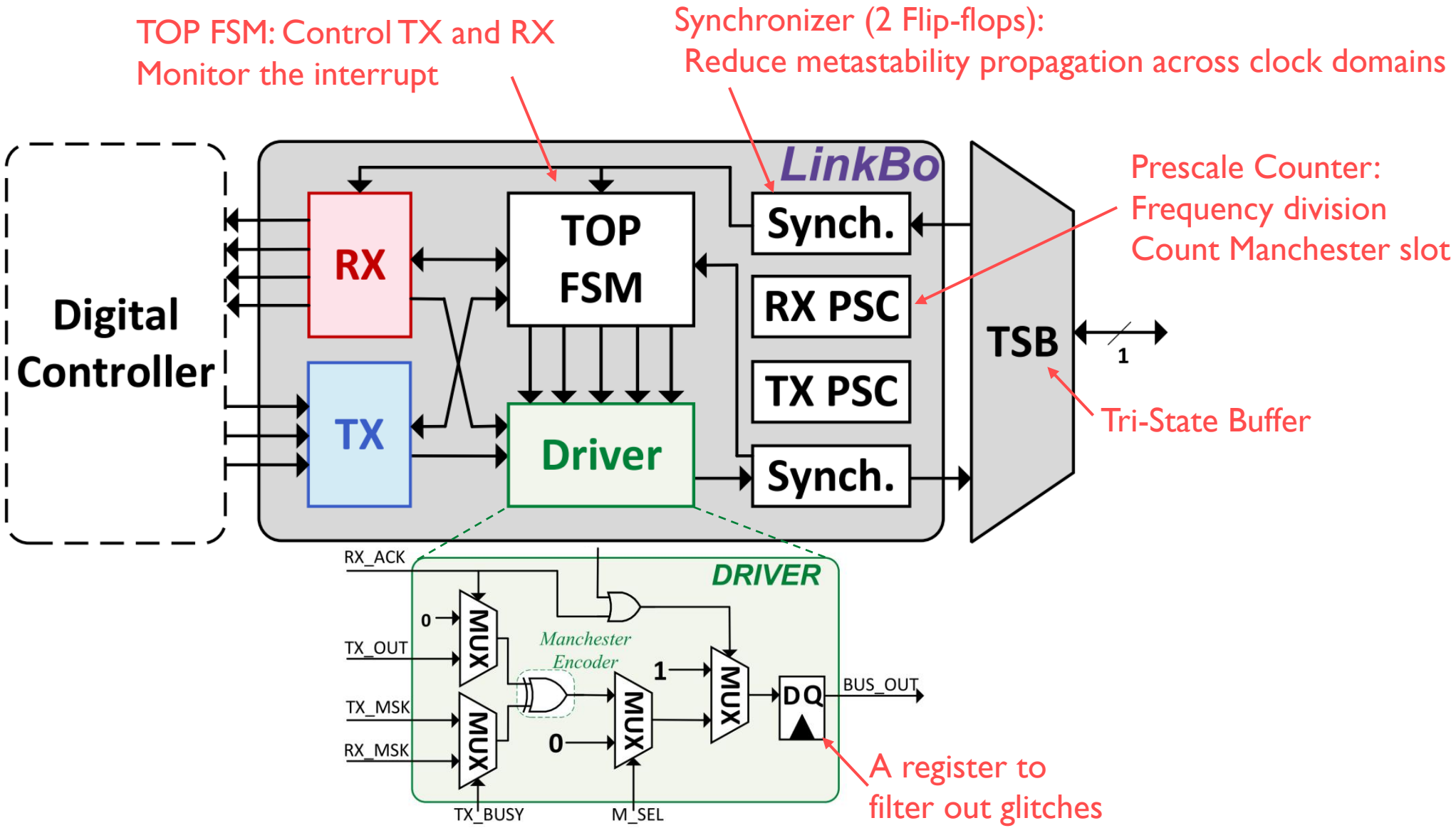




Hardware Architecture

- TOP Level Architecture
- Transmitter (TX)
- Receiver (RX)
- Driver

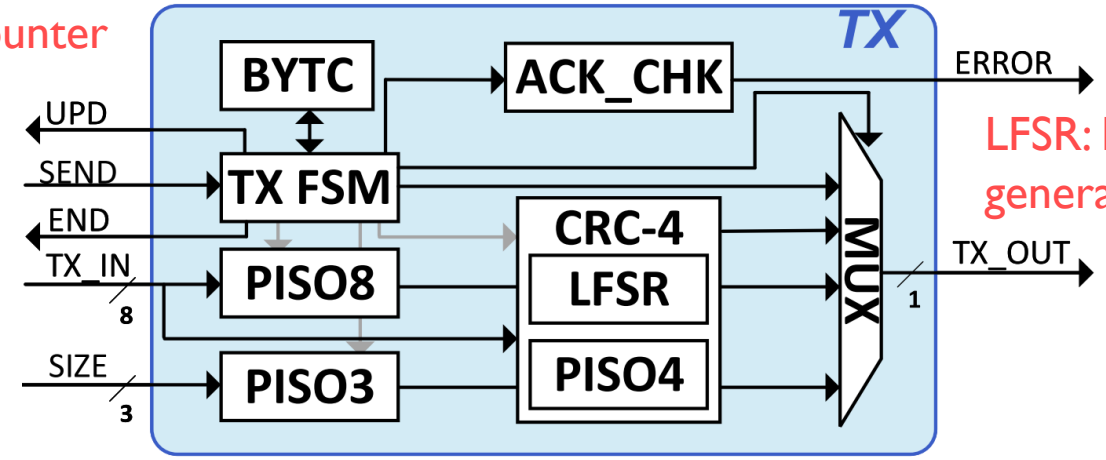
TOP and DriverArchitecture



TX/RX Architecture

ACK Check: check ack and report error

BYTC: Byte Counter

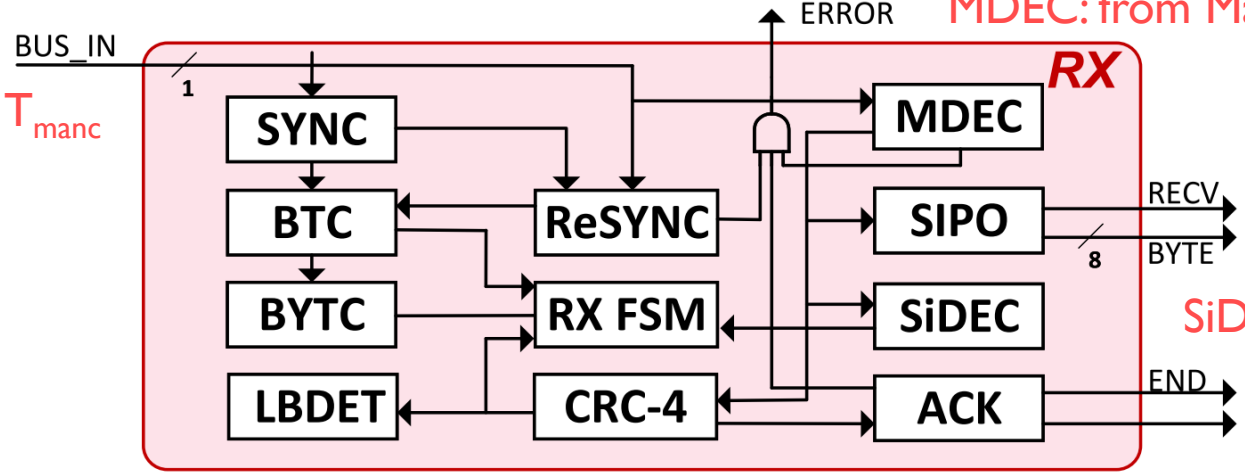


LFSR: Linear-Feedback-Shift-Register, generate CRC

PISO: Parallel In Serial Out

MDEC: from Manchester code to NRZ code.

SYNC:
detect priority and calculate T_{manc}



Re-SYNC:
reset prescaler counter
when bus wrong

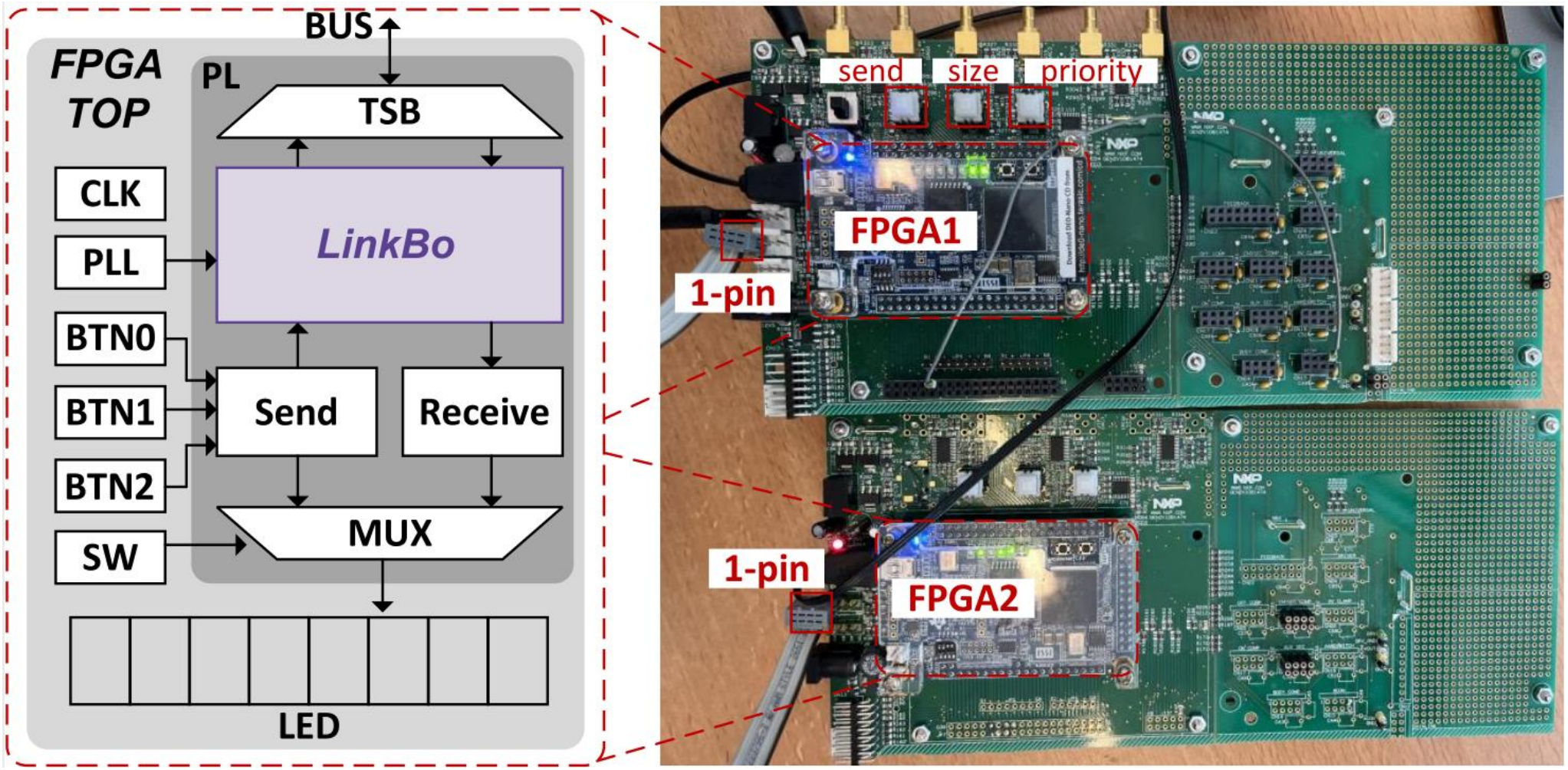
SiDEC: Size decoder.

LowBus Detector (LBDET): Detect high-priority sync interrupt

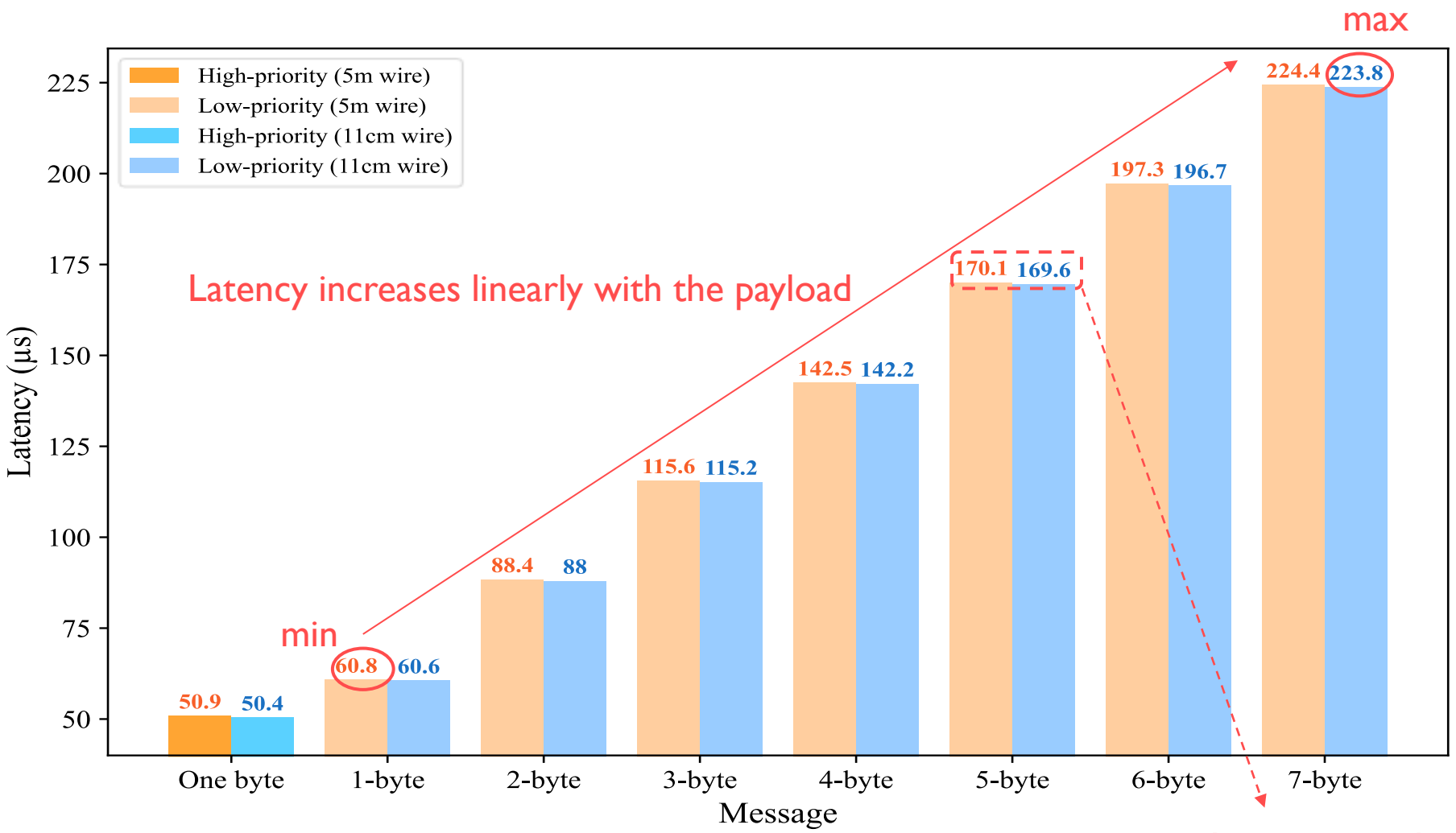
Experiments and Result

- FPGA test
- Latency Analysis
- Sensitivity Analysis
- Protocol Comparison

FPGA Test Setup



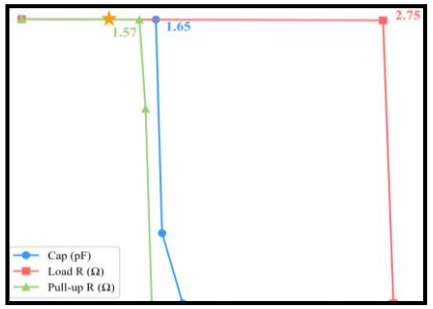
Latency Analysis

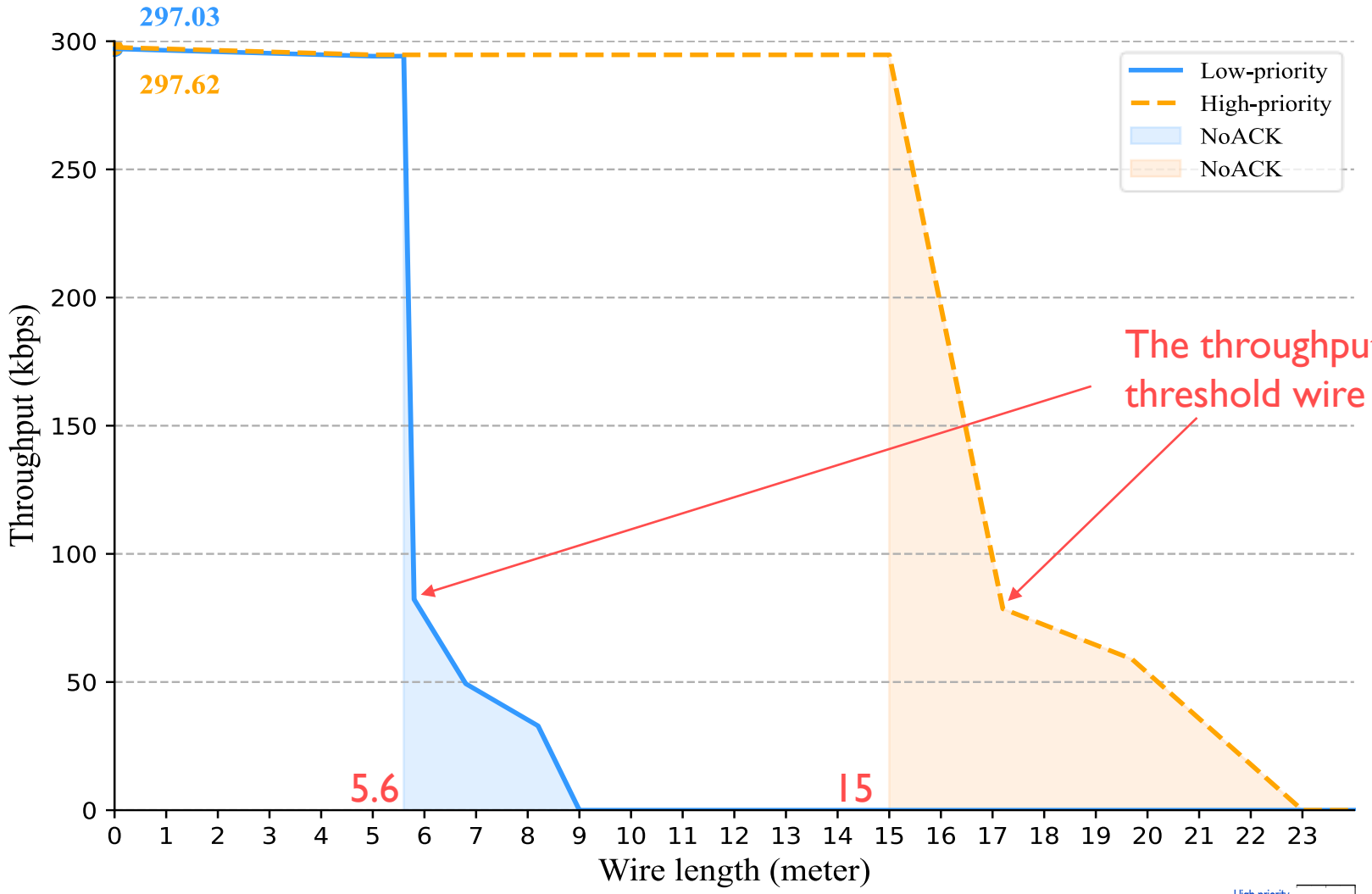


Latency is independent of the wire length !

Sensitivity Analysis

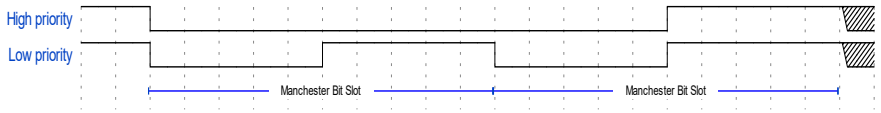
Model Result Recap:





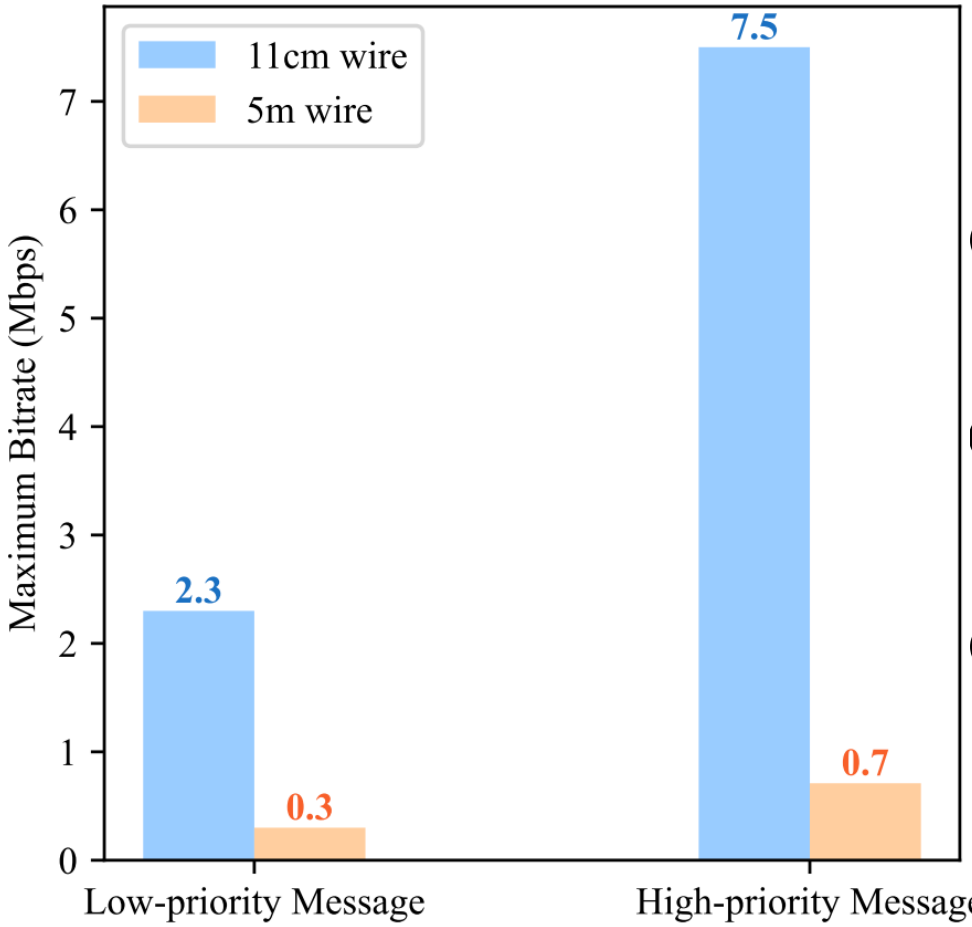
The throughput suddenly drops at a certain threshold wire length

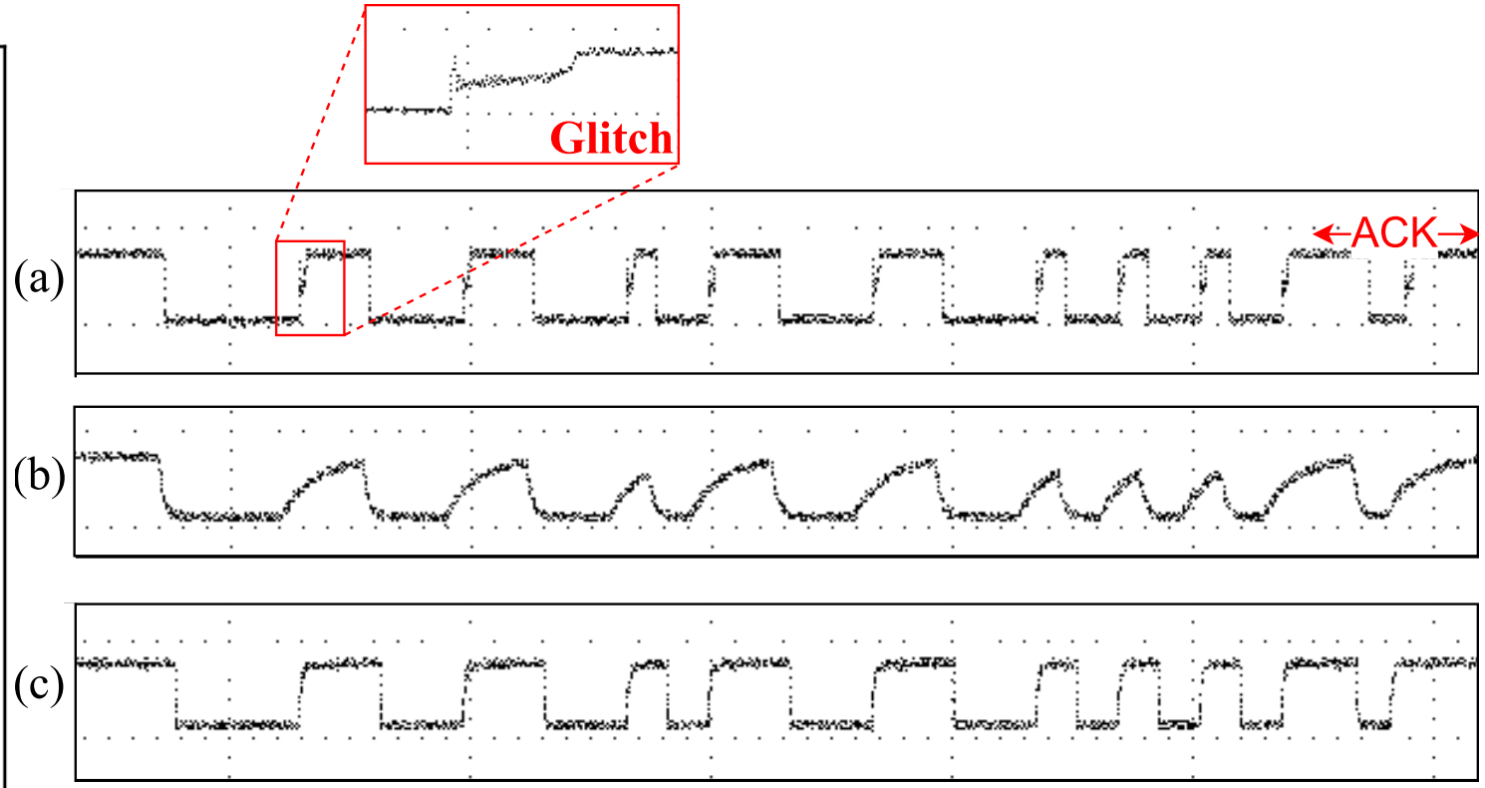
Reason:
High priority message have longer sync field



Bit rate= 300 kbps

Sensitivity Analysis





(a) 14.8 m TX output (b) 14.8m Bus (c) 11cm Bus

High priority can tolerate higher bit rates !
Shorter wire lengths can tolerate higher bit rates !

Protocol Comparison

CLK=3MHz

Protocol	1-wire (TI,ADI)	UNI/O (MicroChip)	LinkBo (our solution)
Type	Asynchronous	Asynchronous	Asynchronous
Duplex	Half Duplex	Half Duplex	Half Duplex
Bit Rate (kbps)	8.33 - 111	10 - 100	294.8 - 297.6
EBR (kbps)	5.8 - 77.2	7.97 - 79.7	158.7 - 252.5
Latency (μs)	1520 - 4480	810 - 1410	50.4 - 223.8
Interrupt	No	No	Yes
Multi-byte	No	Yes, no upper limit	Yes, max 7-byte
CRC	Yes, 8 bits	No	Yes, 4 bits
Acknowledge	No	Yes, 2-bit ack	Yes
Distance (m)	20 - 100	N/A	5.6 - 15

Bit Rate: $R_b = \frac{B_{\text{total}}}{T}$

Effective Bit Rate (EBR): $EBR = \frac{B_{data}}{T}$

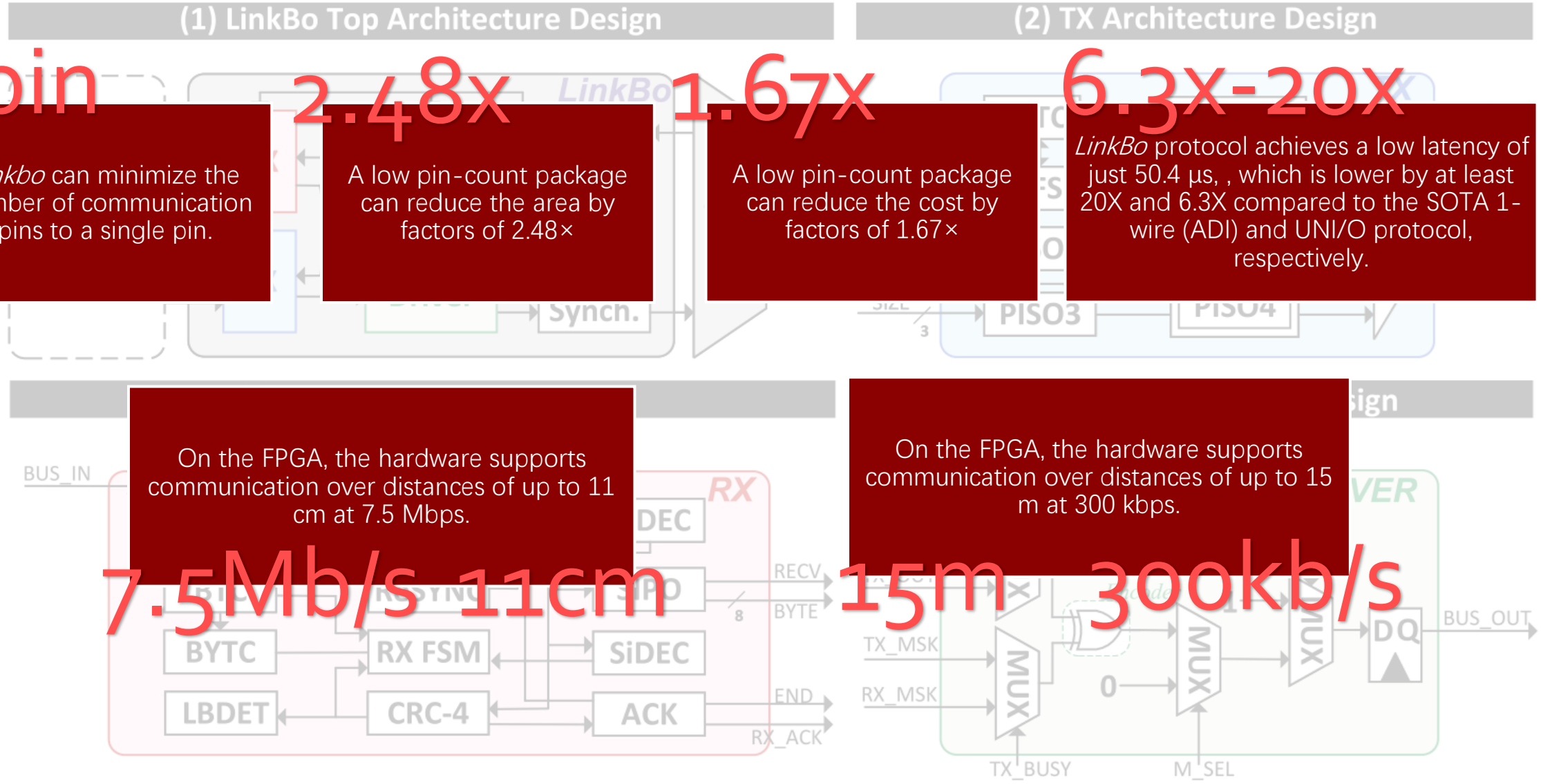
Maximum Latency: time of 7-byte message

Minimum Latency: time of one byte message

Conclusion

- Summary
- Looking Ahead

Summary



1 pin

Linkbo can minimize the number of communication pins to a single pin.

2.48x

A low pin-count package can reduce the area by factors of 2.48×

1.67x

A low pin-count package can reduce the cost by factors of 1.67×

6.3x-20x

LinkBo protocol achieves a low latency of just 50.4 µs, , which is lower by at least 20X and 6.3X compared to the SOTA 1-wire (ADI) and UNI/O protocol, respectively.

On the FPGA, the hardware supports communication over distances of up to 11 cm at 7.5 Mbps.

7.5Mb/s 11cm

On the FPGA, the hardware supports communication over distances of up to 15 m at 300 kbps.

15m 300kb/s

Looking Ahead …

- **Single-wire Protocol for Extreme-Edge Specific Application**
  - Towards an area-efficiency and cost-efficiency *Domain-specific* Application design.
- **Latency and Distance trade-off**
  - Improve distance and decrease latency as much as possible.
- **Multi-device Single-wire Protocol**
  - Explore high-efficient arbitration for multi-drop/peer-to-peer transmission of Single-wire protocol

Thanks !

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